REMARKS/ARGUMENTS

1. In the above referenced Office Action, the Examiner rejected claims 1, 4-16, 19, and 20 under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227) and Tsuji (U.S. Patent No. 5,901,023); and claims 2, 3, 17, and 18 under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227), Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The rejection has been traversed and, as such, the applicant respectfully requests reconsideration of the allowability of claims 1-20.

2. Claims 1, 4-16, 19, and 20 have been rejected under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227) and Tsuji (U.S. Patent No. 5,901,023). The applicant respectfully disagrees with this rejection and the reasoning thereof.

Independent claims 1, 9, and 16 have been amended to include the limitation that an inductor assembly has an inductance value that, at a frequency of the RF signals, resonates with parasitic capacitance of the ESD protection circuitry to provide a low impedance connection at the frequency of the RF signals. As such, the inductor assemblies provide the low frequency connections of the different power supply and/or ground connections and provide, in combination with the parasitic capacitance of the ESD protection circuit, a low impedance path at an RF frequency.

Yue teaches placing an inductor in series with an ESD circuit 40 to produce an ESD protector. (Column 3, lines 50-51) The inductor is effectively acting like a switch to couple the ESD circuit for low frequency signals (e.g., ESD pulses) and to disconnect the ESD circuit 40 for higher frequency signals to effectively eliminate the capacitive load of the ESD circuit 40. (Column 3, line 67, through Column 4, line 11) As such, Yue is teaching that, at the frequency of the higher frequency signals, the inductor in series with the ESD circuit provides a high impedance such that the ESD circuit is disconnected. The opposite of what is presently claimed in claims 1, 9, and 16.

Tsuji teaches placing a first protection circuit 22 for an internal circuit that is coupled to an analog power supply 12, digital power supply line 18, and a digital ground 19; and a second protection circuit 23 for an internal circuit that is coupled to an analog ground 13, the digital power supply line 18, and the digital ground line 19. As such, each protection circuit is coupled to an analog node (e.g., analog power supply or analog ground), the digital power supply line and the digital ground line. As such, Tsuji is teaching having ESD protection between the digital power supply line and the analog power supply line, the digital power supply line and the analog ground, the digital ground and the analog power supply line, and the digital ground and the analog ground in a physical position on the die that was previously unused (column 5, lines 6-13)

Combining the teachings of Woo, Yue, and Tsuji does not render obvious the present claims, especially when Yue teaches the opposite of what is presently claimed. Based on the foregoing, the applicant believes that the present rejection has been overcome.

3. Claims 2, 3, 17, and 18 have been rejected under 35 USC § 103 (a) as being unpatentable over Woo (U.S. Patent No. 6,445,039) in view of Yue (U.S. Patent No. 6,597,227), Kluge (U.S. Patent Application No. 2003/183403) and Tsuji (U.S. Patent No. 5,901,023). The applicant respectfully disagrees with this rejection and the reasoning thereof.

The applicant believes that the above arguments are applicable in distinguishing claims 2, 3, 17, and 18 over the present rejection.

For the foregoing reasons, the applicant believes that claims 1-20 are in condition for allowance and respectfully request that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present invention.

RESPECTFULLY SUBMITTED,

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CERTIFICATE OF MAILING

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